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Optimizing FPGA-based Accelerator Design for Deep ...
ARM Cortex-A9 processor-based SoC FPGAs include a feature called an Accelerator Coherency Port (ACP). Through the ACP, new data produced by an FPGA-based hardware accelerator is transferred directly to the processor’s L2 cache, via a low-latency direct connection (Figure 1). This operation is performed not just quickly, but coherently too.

FPGA-BASED Hardware Accelerators | SpringerLink
At that time, researchers began to notice the FPGA-based neural network accelerator, as shown in Figure 1. Until last year, the number of FPGA-based neural network accelerators published in the IEEE eXplore has reached 69 and is still on the rise. It is enough to illustrate the research trend in this direction.

FPGA-based Accelerator for Long Short-Term Memory ...
DOI: 10.1109/FPL.2016.7577308 Corpus ID: 206657365. A high performance FPGA-based accelerator for large-scale convolutional neural networks @article{Li2016AHP, title={A high performance FPGA-based accelerator for large-scale convolutional neural networks}, author={Huimin Li and Xitian Fan and Li Jiao and Wei Cao and Xuegong Zhou and Lingli Wang}, journal={2016 26th International Conference on ...

Fundamentals of FPGA Based Acceleration
The techniques investigated in this paper represent the recent trends in FPGA-based accelerators of deep learning networks. Thus, this review is expected to direct the future advances on efficient hardware accelerators and to be useful for deep learning researchers.

A high performance FPGA-based accelerator for large-scale ...
exibility into consideration, an FPGA-based accelerator is a good choice, and previous de-signs have showed great bene ts brought by FPGA-based accelerators[5][10][17]. Typically in practice, an LSTM-RNN model must be trained o -line for a fairly good prediction accuracy, then it can be applied to various real-life applications. As a

FPGA-based Accelerator for Long Short-Term Memory ...
throughput of an FPGA-based accelerator. In this work, an entire CNN model is proposed consisting of all CNN layers: convolution, normalization, pooling, and classification layers. Work [26] proposes a FPGA accelerator with a scalable architecture of deeply pipelined Open CL kernels.

FPGA-Based CNN Inference Accelerator Synthesized from ...
Based on a Xilinx Spartan 6 FPGA, the XJAccelerator card is principally designed to provide a versatile platform for accelerated programming applications. In this mode the FPGA is configured with XJFlash to program flash devices connected to any of the three I/O headers.

Introduction to FPGA-Based Accelerators | element14 | FPGA ...
LSTM on FPGA.“ International Symposium on FPGA 2017. [Link] Genomic Analysis 80x Edico Genome. "DRAGEN Genome Pipeline." Last accessed April 6, 2017. [Link] Pattern Matching 18x Shreyas G Singapura et al. "FPGA Based Accelerator for Pattern Matching in YARA Framework.“ CENG 2015. [Link]

XJAccelerator — FPGA based programming - XJTAG
Design and Evaluation of FPGA Based Hardware Accelerator for Elliptic Curve Cryptography Scalar Multiplication

Hardware Acceleration in SoC FPGAs
The book is intended to be a valuable support material for university and industrial engineering courses that involve FPGA-based circuit and system design. Keywords. FPGA Optimization Techniques Data Processing Combinatorial Optimization Hardware Accelerators Xilinx .

GitHub - thedatabusdotio/fpga-ml-accelerator: This ...
An FPGA-based CNN accelerator synthesized from multi-threaded (Pthreads) C software. The software behavior closely resembles the synthesized hardware, easing design and debugging by allowing it to proceed in software. Generation and exploration of accelerator architectural variants via software/constraint changes alone.

fpga-accelerator · GitHub Topics · GitHub
This repository hosts the code for an FPGA based accelerator for convolutional neural networks

[PDF] A high performance FPGA-based accelerator for large ...
An OpenCL-based FPGA Accelerator for Convolutional Neural Networks. deep-neural-networks fpga deep-learning hls hardware opencl altera-opencl-sdk fpga-accelerator Updated Jul 28, 2020; C; google / qkeras Star 215 Code Issues Pull requests QKeras: a ...

[1901.00121] FPGA-based Accelerators of Deep Learning ...
This work proposes an end-to-end FPGA-based CNN accelerator with all the layers mapped on one chip so that different layers can work concurrently in a pipelined structure to increase the throughput. A methodology which can find the optimized parallelism strategy for each layer is proposed to achieve high throughput and high resource utilization.

A Survey of FPGA Based Deep Learning Accelerators ...
This paper proposes an FPGA-based training accelerator utilizing a sparseness of a CNN, which consists of universal convolutional units and pooling units with distributed stacks. The proposed universal convolution architecture supports various convolution operations, such as the point-wise, depth-wise, large kernel and atrous convolutions used in the modern CNN.

Design and Evaluation of FPGA Based Hardware Accelerator ...
speeding up the feedforward computation with FPGA based accelerator design. A typical CNN is composed of two components: a feature extractor and a classi er. The feature extractor is used to lter input images into\feature maps"that represent various features of the image. These features may include corners,

An Fpga Based Accelerator For
The recently launched BittWare 250-M2D is an FPGA-based Computational Storage Processor (CSP) designed to meet the draft M.2 Accelerator Module Hardware Specification standard. It is intended to operate in Glacier Point carrier cards for Yosemite servers.

An FPGA-Based CNN Accelerator Integrating Depthwise ...
FPGA. The FPGA board we use is Xilinx VC707, which has a Xilinx Virtex7-485t FPGA chip on it. The working frequency of the accelerator is set to 150MHz. For per-formancecomparison,wealsohaveasoftwareimplemen-tation of LSTM-RNN inference, which runs on an Intel XeonCPUE5-2430. TheworkingfrequencyofthisCPU is2.20GHz. B. Experimental Results