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bindkeys is the fastest  
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requires a degree of  
familiarity with  
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environment. 3.  
Typing the



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corresponding skill function at the prompt in the CIW. This is an advanced way of invoking commands in Cadence and requires familiarity with the Cadence Design System and with the skill functions.

TUTORIAL  
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a. Continue working in the same project directory as the earlier tutorial. The directory is called 'tut\_65nm' in this tutorial. b. Make sure you have copied rtl.tcl from the earlier tutorial. You can find the link here: [rtl.tcl](#). This is the source script that has library path, path to Verilog script,

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synthesis commands.

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Tutorial D Using  
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Tutorial D: Design  
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2. Running a  
Parametric Analysis

This part of the  
tutorial will show you  
how to set up a  
simple parametric

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sweep analysis in  
Cadence. In this  
example, the width of  
the PMOS transistor  
is ...

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5. ANALOG DESIGN  
WITH CADENCE  
DESIGN

FRAMEWORK II Now  
we are going to

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illustrate how to carry out the complete design flow shown in Fig. 1 using the Cadence tools. A simple inverter will be designed using the AMI 0.5 $\mu$ m CMOS technology. However, the same procedures apply to complete chip designs. 5.1. Library creation and selection of

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TUTORIAL

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The objective is to give a tutorial to circuit designers who would like to get acquainted with Cadence design tools (version 5.1.4.1) for VLSI custom design. A step by step tutorial



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approach is adopted.

## Front End Design

Using Cadence Tool -  
Part 02 Synthesis (rc

...

Cadence Tutorial for  
Cadence version 6.1  
Inkwon Hwang Feb,  
2010 1. ... Design flow  
of layouts is very  
similar to one of  
schematics, but it has  
additional step which

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is LVS check. It is for  
check if your layout is  
identical to the  
schematic or not.  
Hence, this step is  
very

Cadence |  
Computational  
Software for  
Intelligent System ...  
Layout of CMOS  
Inverter

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CESCA - VLSI  
Design: Cadence  
Tutorial

Welcome all, this is my first video here on Youtube. In this video, we will talk about the steps of designing a CMOS inverter in Cadence Virtuoso Analog Envi...

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VLSI Design I using  
Cadence This tutorial

has been adapted

from EE5323 offered

in Fall 2007. Thanks

to Jie Gu, Prof. Chris

Kim and Satish

Sivaswamy of the

University of

Minnesota for creating

& updating this

tutorial. Thanks are

also due to NCSU

wiki for parts of the

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layout section. Setting  
up your Account

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[www.vtvt.ece.vt.edu](http://www.vtvt.ece.vt.edu) .

To get you acquainted with the layout process, a tutorial has been developed that describes the procedure to custom layout an inverter.

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You can use this tutorial to perform all the steps in the PCB design process. The tutorial focuses on the sequence of steps to be performed in the PCB design cycle for an electronic design, starting with capturing the electronic circuit,



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simulating the design with PSpice, through the PCB layout stages, and finishing with the processing of the manufacturing output and maintaining the design ...

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*Page 25/31*

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assumed to be a constant value and therefore the values for the areas and perimeters do not change. This is a flaw in the NCSU implementation.

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*Page 26/31*

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d) Add wires to connect gates and pins: Add -> Wire or use the toolbar. Use Check and Save to save design. Select Design -> Check and Save or use the toolbar. Errors will be displayed in the CIW. Correct any errors. Further instruction is available in cdsdoc.

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tutorial:

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characterization.

Design Systems

Fig. 1 shows the basic design flow of an analog IC design, together with the Cadence tools required in each step.

First, a schematic view of the circuit is created using the Cadence Composer

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Schematic Editor.

Alternatively, a text netlist input can be employed. Then, the circuit is simulated using the Cadence Affirma analog

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