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cache ,the latencies  
(in CPU cycles) of  
different kinds of  
access are follows:

cache hit , 1 cycle

;cache miss,105 cycle;

main memory access  
with cache disable

,100 cycles a.) when

you run a program  
with an overall miss

rate of 5% what will  
the avg. memory ...

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Appendix C, and we will see examples when we examine the implementation of the multicycle controller in Section D.3. Elaboration: In general, a logic equation and truth table representation

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of a logic function are equivalent. (We discuss this in further detail in Appendix C.) However, when a

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the solution shown in  
Figure C11 | The  
branch penalty is fixed  
and cannot be

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a modern computer

are digital. Digital

electronics operate

with only two voltage

levels of interest: a

high voltage and a

low voltage. ... C-6

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logic equations for the logic functions, D, E, and F, described in the previous example.

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16.(page C16) 1.  
solution point 2.

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graph 3. Algebraic,  
graphical, numerical

4. 1. If possible,

rewrite the equation

so that one of the

variables is isolated

on one side of the

equation. 2. Make a

table of values

showing several

solution points. 3.

Plot these points on a

rectangular

coordinate system. 4.

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