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CHAPTER 2 COMPUTER EVOLUTION AND PERFORMANCE

ANSWERS TO QUESTIONS 2.1 In a stored program computer, programs are represented in a form suitable for storing in memory alongside the data.

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architectural specifications.

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- 13 - 2.9 When the parallel load input = 1,

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the clock pulses go through the AND gate and the data inputs are loaded into the register when the parallel load input = 0, the output of

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INTR is a signal which if enabled then
microprocessor has interrupt enabled it
receives high INR signal & activates INTA
signal, so another request can't be accepted
till CPU is busy in servicing interrupt.
Hence (A) is correct option. Question. 12

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