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ANSWERS TO QUESTIONS

- 13 - 2.9 When the parallel load input = 1, the clock pulses go through the AND gate and the data inputs are loaded into the register when the parallel load input = 0, the output of

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Computer Organization & Architecture SOLUTION INTR is a signal which if enabled then microprocessor has interrupt enabled it receives high INTR signal & activates INTA signal, so another request can't be accepted till CPU is busy in servicing interrupt. Hence (A) is correct option. Question. 12

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