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What is Signal?
Impact of Digital Control in Power Electronics Dragan Maksimovi´c, Regan Zane and Robert Erickson Colorado Power Electronics Center Department University of Colorado, Boulder, CO 80309-0425 Email: fmaksimov, zane, rweg@colorado.edu Abstract—In this paper, we di impact of digital

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Lecture 17 - S-R,J-K and D Flip Flops

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J&D Electronics

Digital Electronics is an important subject, common for Electrical, Electronics, and Instrumentation Engineering students. It deals with the practical knowledge of Digital Systems and how they are implemented in various digital instruments.

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FLIP-FLOPS

When $J = 0$ and $K = 0$. These J and K inputs disable the NAND gates, therefore clock pulse have no effect on the flip flop. In other words last value. When $J = 0$ and $K = 1$, The upper NAND gate is disabled the lower NAND gate is enabled if Q is 1 therefore, flip flop will be reset (=1)if not already in that state.

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