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Abstract: This paper examines the apparent limits, possible extensions, and applications of CMOS technology in the nanometer regime. Starting from device scaling theory and current industry projections, we analyze the achievable

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performance and possible limits of CMOS technology from the point of view of device physics, device technology, and power consumption.

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on Power Performance
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NANOARCH is the annual cross-disciplinary forum for the discussion of novel post-CMOS nanocomputing directions and emerging nanoscale CMOS. The symposium seeks papers on innovative ideas for solutions to the principal challenge

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facing integrated
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Compact modeling of
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Design, reliability, and
scaling trend February
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and Applications,
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The scaling of
MOSFET causes
various process
variations and defects
which result in
increasing performance
loss of nanoscale

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integrated circuits.

Major sources of process variations and defects in nanometer CMOS technology are studied. Then, their impact on MOSFET characteristics and on VCO circuit performances is analyzed. Finally, the paper proposes...

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low temperature:
Design, reliability ...
Lewynet al.: Analog
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precharging in high-
performance nanoscale

...

Shailendra Jain, et al.,
"A 280mV-to-1.2V wide-
operating-range IA-32
processor in 32nm
CMOS," Solid-State
Circuits Conference
Digest of Technical
Papers {ISSCC}, 2012
IEEE International, pp.
66--68, 2012 Google
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Steven Hsu, et al., "A
280mV-to-1.1V 256b
reconfigurable SIMD
vector permutation
engine with
2-dimensional shuffle
in 22nm CMOS," Solid-
State Circuits
Conference ...

in Proceedings of IEEE
International
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Abstract: Well-designed

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The Insulating layer between the increasingly unruly behavior of scaled complementary metal-oxide-semiconductor devices and the systems we seek to construct from them. As we move forward into the nanoscale regime, circuit design is burdened to

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Idquohiderdquo more
of the problems
intrinsic to deeply
scaled devices.

Digital Circuit Design
Challenges and
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This book describes methodologies in the design of VLSI devices, circuits and their applications at nanoscale levels. The book begins with the discussion on the dominant role of power dissipation in highly scaled devices. The 15 Chapters of the book are classified under

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four sections that cover
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design, modeling, and
simulation

Near-threshold voltage
design in nanoscale
CMOS ...

Greeshma.v and Udaiya
R Kumar. Article:

Certain Investigations
on Power Performance
in Nanoscale CMOS
Digital Circuits with
Low Leakage Design

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and Communication
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ICIIECS(4):6-9,
November 2014. Full
text available.

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However, current PA designs in nanometer and micrometer complementary metal-oxide semiconductor (CMOS) technology present inevitable drawbacks, such as oxide breakdown and hot electron effect. A well-defined architecture, including a linear and simple functional block

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synthesis, is critical in
designing CMOS PA
for various
applications.

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nanoscale CMOS are
examined, with a view
to better defining the
likely capabilities of
future microelectronic
systems. ...

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THE IEEE, VOL. 87,
NO. 4, APRIL 1999
537. Table 1

Technology Scaling
Rules for Three Cases (α)
Is the Dimensional
Scaling Parameter, Is
the

FinFETs for nanoscale
CMOS digital
integrated circuits ...

Ye, Y, Zhu, Y, He, H,

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Mei, J, Cao, Y & He, J
2013, Compact
modeling of parameter
variations of nanoscale
CMOS due to random
dopant fluctuation. in
Technical Proceedings
of the 2013 NSTI
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NSTI-Nanotech 2013.
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Conference and Expo,
NSTI-Nanotech 2013,
vol. 2, pp. 552-555,
Nanotechnology 2013:
Electronics ...

CMOS Compatible
Nanoscale Nonvolatile
Resistance Switching ...
High-performance
caches statically pull up
the bit-lines in all cache
subarrays to optimize
cache access latency.

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Unfortunately, such architecture results in a significant waste of energy in nanoscale CMOS implementations due to high leakage and bitline discharge in the unaccessed subarrays. Recent research advocates bitline isolation to control precharging of individual subarrays using ...

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techniques employed.

These two-terminal
resistance switching
devices show excellent
scaling potential well
beyond 10 Gb/cm^2 and
exhibit high yield
(99%), fast
programming speed (5
ns), high on/off ratio
(10^3 ...

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Nanoscale computing systems show great potential but at the same time introduce new challenges not encountered in the world of conventional CMOS designs and manufacturing. For example, these systems need to work around layout and doping

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constraints resulting from unconventional bottom-up selfassembly, and need to cope with high manufacturing defect rates and transient faults.

Electronics | Special
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CMOS Technologies
As complementary meta
l-oxide-semiconductor
(CMOS) technologies

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are scaled down into the nanometer range, a number of major nonidealities must be addressed and overcome to achieve a successful analog and physical circuit design. The nature of these nonidealities has been well reported in the technical literature. They include hot carrier injection and

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time-dependent
dielectric breakdown
effects ...

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